

# Introduction to Formal Methods

# Lecture 11 Hoare Logic for Concurrent Programs Hossein Hojjat & Fatemeh Ghassemi

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• Is the following true?

 $\begin{cases} x = 0 \\ y := x; \\ x := x + 1; \\ \{ x = 1 \land y = 0 \} \end{cases}$ 

• YES!

• Is the following still true?

 $\{x = 0\} \\ y := x; \\ x := x + 1; \\ \{x = 1 \land y = 0\}$  x := 5;

• Is the following still true?

 $\{x = 0\} \\ y := x; \\ x := x + 1; \\ \{x = 1 \land y = 0\}$  x := 5;

• NO!

• Is the following still true?

 $\{x = 0\}$ y := x;  $\{x + 1 = 1 \land y = 0\}$ x := x + 1;  $\{x = 1 \land y = 0\}$ () x := 5;

• NO!

• Is the following still true?

$$\{x = 0\} \\ y := x; \\ x = x + 1; \\ \{x = 1 \land y = 0\}$$
   
 x := x + 1;   
 {x = 1 \land y = 0}

- NO!
- The parallel process may interfere with the intermediate assertions

• Extend the language of previous lectures with parallel composition

• Can we derive a Hoare triple for parallel composition from the triples of each command?

First Attempt:

$$\vdash \{P_1\} c_1 \{Q_1\} \vdash \{P_2\} c_2 \{Q_2\} \\ \vdash \{P_1 \land P_2\} c_1 \parallel c_2 \{Q_1 \land Q_2\}$$

• Intuition: if we satisfy the preconditions of  $c_1$  and  $c_2$ , their postconditions will be satisfied too

## **Unsoundness of First Attempt**

$$\frac{\vdash \{P_1\} c_1 \{Q_1\} \vdash \{P_2\} c_2 \{Q_2\}}{\vdash \{P_1 \land P_2\} c_1 \parallel c_2 \{Q_1 \land Q_2\}}$$

• This rule is not always sound, consider:

 $\{x=1\} \ y:=0 \ \{x=1\} \qquad \qquad \{\textit{true}\} \ x:=10 \ \{\textit{true}\}$ 

• It does not hold that

 $\{x = 1 \land \mathsf{true}\} \quad y := 0 \parallel x := 10 \quad \{x = 1 \land \mathsf{true}\}$ 

 $\frac{\vdash \{P_1\} c_1 \{Q_1\} \vdash \{P_2\} c_2 \{Q_2\}}{\vdash \{P_1 \land P_2\} c_1 \parallel c_2 \{Q_1 \land Q_2\}}$ 

- If  $c_1$  and  $c_2$  do not read and write the same variables, and all the pres- and post- conditions talk about different variables
- What's wrong with this?

 $\frac{\vdash \{P_1\} c_1 \{Q_1\} \quad \vdash \{P_2\} c_2 \{Q_2\}}{\vdash \{P_1 \land P_2\} c_1 \parallel c_2 \{Q_1 \land Q_2\}}$ 

- If  $c_1$  and  $c_2$  do not read and write the same variables, and all the pres- and post- conditions talk about different variables
- What's wrong with this?
- No way to prove some program
- The rule is **incomplete**

$$\vdash \{P_1\} c_1 \{Q_1\} \vdash \{P_2\} c_2 \{Q_2\} \\ \vdash \{P_1 \land P_2\} c_1 \parallel c_2 \{Q_1 \land Q_2\}$$

- If a command does not modify any variable from the pre-condition of the other triple
- Let UPD(c) be the set of variables that are updated (modified) in c  $FV(P_1) \cap UPD(c_2) = \emptyset$  $FV(P_2) \cap UPD(c_1) = \emptyset$

$$\vdash \{P_1\} c_1 \{Q_1\} \vdash \{P_2\} c_2 \{Q_2\} \\ \vdash \{P_1 \land P_2\} c_1 \parallel c_2 \{Q_1 \land Q_2\}$$

- If a command does not modify any variable from the pre-condition of the other triple
- Let UPD(c) be the set of variables that are updated (modified) in c  $FV(P_1) \cap UPD(c_2) = \emptyset$  $FV(P_2) \cap UPD(c_1) = \emptyset$
- Still incomplete: cannot prove

$$\{x = 0\} \\ x := x + 1 \parallel x := x + 2 \\ \{x = 3\}$$

# $\frac{\vdash \{P_1\} c_1 \{Q_1\} \vdash \{P_2\} c_2 \{Q_2\}}{\vdash \{P_1 \land P_2\} c_1 \parallel c_2 \{Q_1 \land Q_2\}}$

 $\mathsf{If} \ \mathit{UPD}(c_1) \cap (\mathit{FV}(P_2) \cup \mathit{FV}(Q_2)) = \emptyset \ \mathsf{and} \ \mathit{UPD}(c_2) \cap (\mathit{FV}(P_1) \cup \mathit{FV}(Q_1)) = \emptyset$ 

$$\frac{\vdash \{P_1\} c_1 \{Q_1\} \vdash \{P_2\} c_2 \{Q_2\}}{\vdash \{P_1 \land P_2\} c_1 \parallel c_2 \{Q_1 \land Q_2\}}$$

If  $UPD(c_1) \cap (FV(P_2) \cup FV(Q_2)) = \emptyset$  and  $UPD(c_2) \cap (FV(P_1) \cup FV(Q_1)) = \emptyset$ Still unsound. Consider:

$$\{x=0\} \ y:=x; z:=y \ \{z=0\} \qquad \qquad \{\textit{true}\} \ y:=10 \ \{\textit{true}\}$$

It does not hold that

 $\{x = 0 \land true\} \ y := x; z := y \parallel y := 10 \ \{z = 0 \land true\}$ 

**Diagnose:** y := 10 interferes with the proof of

$$\{x = 0\} \ y := x; z := y \ \{z = 0\}$$
$$y \stackrel{\uparrow}{=} 0$$

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• Susan Owicki,

"Axiomatic proof techniques for parallel programs", Cornell University, Ithaca, NY, 1975

- Under supervision of Prof. David Gries
- First complete logic for partial correctness of concurrent programs that communicate using shared variables

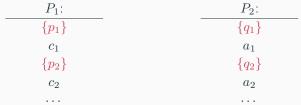




# Interference Freedom

• Interference Freedom: every assertion used in the local verification

is not invalidated by the execution of the other process



We say that they are interference free iff

 $\begin{aligned} \forall p_i \in \text{assertions of } P_1 \land \forall a_j \in \text{atomic actions of } P_2, \\ & \{p_i \land \text{pre } a_j\} \\ & a_j \\ & \{p_i\} \\ & (\text{and vice versa}) \end{aligned}$ 

• If  $P_1$  has n statements and  $P_2$  has m statements, proving interference freedom requires proving  $O(n \times m)$  correctness formulas

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 $\begin{array}{rrr} \vdash & \{P_1\} \ c_1 \ \{Q_1\} \\ & \vdash \ \{P_2\} \ c_2 \ \{Q_2\} \end{array} \\ \\ \begin{array}{rrr} \mbox{the two proofs are non-interfering} \\ \hline & \vdash \ \{P_1 \land P_2\} \ c_1 \parallel c_2 \ \{Q_1 \land Q_2\} \end{array} \end{array}$ 

# Example

- These two proof outlines are correct but not interference free
- For example, the assertion x = 0 is not preserved against the atomic action x := x + 2

$$\begin{array}{ll} \{x=0\} & \{ \textit{true}\} & \{x=0 \land x=0\} \\ x:=x+2; & || & x:=0; & x:=x+2; \\ \{x=2\} & | & \{x=0\} & \{x=0\} \end{array}$$

• By weakening the postconditions we obtain both correct and interference free proof outlines:

$$\begin{cases} x = 0 \} & \{ true \} & \{ (x = 0 \lor x = 2) \land x = 0 \} & \{ x = 0 \} \\ x := x + 2; & x := 0; & x := x + 2; \\ \{ x = 0 \lor x = 2 \} & \{ x = 0 \lor x = 2 \} & \{ x = 0 \lor x = 2 \} & x := x + 2; \\ \{ x = 0 \lor x = 2 \} & \{ x = 0 \lor x = 2 \} & x := x + 2; \\ \{ x = 0 \lor x = 2 \} & \{ x = 0 \lor x = 2 \} & x := x + 2; \\ \{ x = 0 \lor x = 2 \} & x :=$$

# Completeness

• Can you prove the following?

$$\{x = 0\}$$

$$x := x + 1$$

$$\{x = 2\}$$

## Completeness

- Can you prove the following?
- We can prove something weaker

$$\begin{cases} x = 0 \lor x = 1 \\ x := x + 1 \\ \{x = 1 \lor x = 2 \} \end{cases}$$

$$\begin{cases} x = 0 \lor x = 1 \\ \\ x := x + 1 \\ \{x = 1 \lor x = 2 \} \end{cases}$$

$$\{x = 1 \lor x = 2 \}$$

- But how can we derive the postcondition x = 2?
- We need **auxiliary** variables:
- Variables that do not affect the control flow nor the data flow of the other variables, but record information useful for the proof

Add two auxiliary variables a and b: Represent the contribution of each thread to x

 $\{x = 0\} \\ (a, b) := (0, 0)$ 

$$(x,a) := (x+1,1)$$
 ||  $(x,b) := (x+1,1)$   
 $\{x = 2\}$ 

 $(x_1, x_2) := (e_1, e_2)$  atomic parallel assignment

Add two auxiliary variables a and b: Represent the contribution of each thread to x

$$\{x = 0\} \\ (a,b) := (0,0) \\ \{x = a + b \land a = 0 \land b = 0\} \\ \{x = a + b \land a = 0\} \\ (x,a) := (x + 1, 1) \\ \{x = a + b \land a = 1\} \\ \{x = 2\}$$
 
$$\{x = 0\} \\ \{x = 0, 0 \land b = 0\} \\ \{x = a + b \land b = 0\} \\ \{x = a + b \land b = 1\} \\ \{x = 2\}$$

 $(x_1, x_2) := (e_1, e_2)$  atomic parallel assignment

#### Horn Clauses for Concurrent Counters

Global Variable: n

#### Left Thread

#### **Right Thread**

$$\begin{array}{ccccc} n = 0 & \rightarrow & P_1(n) & n = 0 & \rightarrow & Q_1(n) \\ P_1(n) \wedge n' = n + 1 & \rightarrow & P_2(n') & Q_1(n) \wedge n' = n - 1 & \rightarrow & Q_2(n') \\ P_2(n) \wedge n' = n - 1 & \rightarrow & P_1(n') & Q_2(n) \wedge n' = n + 1 & \rightarrow & Q_1(n') \end{array}$$

 $Q_2(n) \wedge P_2(n) \wedge (n=0) \rightarrow false$ 

#### Horn Clauses for Concurrent Counters

Global Variable: n

Left Thread

**Right Thread** 

$$\begin{array}{ccccc} n = 0 & \rightarrow & P_1(n) & n = 0 & \rightarrow & Q_1(n) \\ P_1(n) \wedge n' = n + 1 & \rightarrow & P_2(n') & Q_1(n) \wedge n' = n - 1 & \rightarrow & Q_2(n') \\ P_2(n) \wedge n' = n - 1 & \rightarrow & P_1(n') & Q_2(n) \wedge n' = n + 1 & \rightarrow & Q_1(n') \end{array}$$

$$Q_2(n) \wedge P_2(n) \wedge (n=0) \rightarrow false$$

**Unsound:** proves to be correct although the real system does not have the property

$$P_1(n) \equiv (n=0) \qquad P_2(n) \equiv (n=1) \qquad Q_1(n) \equiv (n=0) \qquad Q_2(n) \equiv (n=-1)_{11}$$

# **Owicki-Gries Interference-Free Conditions**

Global Variable: n

$$\begin{split} P_1(n,1) \wedge Q_1(n,1) \wedge n' &= n+1 \rightarrow Q_1(n',2) \\ P_1(n,2) \wedge Q_2(n,1) \wedge n' &= n+1 \rightarrow Q_2(n',2) \\ P_2(n,1) \wedge Q_1(n,2) \wedge n' &= n-1 \rightarrow Q_1(n',1) \\ P_2(n,2) \wedge Q_2(n,2) \wedge n' &= n-1 \rightarrow Q_2(n',1) \\ Q_1(n,1) \wedge P_1(n,1) \wedge n' &= n-1 \rightarrow P_1(n',2) \\ Q_1(n,2) \wedge P_2(n,1) \wedge n' &= n-1 \rightarrow P_2(n',2) \\ Q_2(n,1) \wedge P_1(n,2) \wedge n' &= n+1 \rightarrow P_1(n',1) \\ Q_2(n,2) \wedge P_2(n,2) \wedge n' &= n+1 \rightarrow P_2(n',1) \end{split}$$

#### **Owicki-Gries Interference-Free Conditions**

Global Variable: n

$$\begin{split} P_1(n,1) \wedge Q_1(n,1) \wedge n' &= n+1 \rightarrow Q_1(n',2) \\ P_1(n,2) \wedge Q_2(n,1) \wedge n' &= n+1 \rightarrow Q_2(n',2) \\ P_2(n,1) \wedge Q_1(n,2) \wedge n' &= n-1 \rightarrow Q_1(n',1) \\ P_2(n,2) \wedge Q_2(n,2) \wedge n' &= n-1 \rightarrow Q_2(n',1) \\ Q_1(n,1) \wedge P_1(n,1) \wedge n' &= n-1 \rightarrow P_1(n',2) \\ Q_1(n,2) \wedge P_2(n,1) \wedge n' &= n-1 \rightarrow P_2(n',2) \\ Q_2(n,1) \wedge P_1(n,2) \wedge n' &= n+1 \rightarrow P_1(n',1) \\ Q_2(n,2) \wedge P_2(n,2) \wedge n' &= n+1 \rightarrow P_2(n',1) \end{split}$$

# Monolithic Encoding

#### Global Variable: n

- Uses only one relation symbol to model the system:  $\mathbf{R}(id, n, t_1, t_2)$
- Invariant covering the whole system
- Simpler and creates more elegant solutions

$$\begin{array}{lll} (n=0) \wedge (t_1=1) \wedge (t_2=1) & \to & \mathbf{R}(id,n,t_1,t_2) \\ \mathbf{R}(1,n,1,t_2) \wedge (n'=n+1) & \to & \mathbf{R}(1,n',2,t_2) \\ \mathbf{R}(1,n,2,t_2) \wedge (n'=n-1) & \to & \mathbf{R}(1,n',1,t_2) \\ \mathbf{R}(2,n,t_1,1) \wedge (n'=n-1) & \to & \mathbf{R}(2,n',t_1,2) \\ \mathbf{R}(2,n,t_1,2) \wedge (n'=n+1) & \to & \mathbf{R}(2,n',t_1,1) \end{array}$$

# **Monolithic Encoding**

#### Global Variable: n

#### **Interference-Free Conditions**

 $\begin{array}{rrrr} \vdash & \{P_1\} \ c_1 \ \{Q_1\} \\ \vdash & \{P_2\} \ c_2 \ \{Q_2\} \\ \hline \\ interference \ freedom \\ \hline \\ \vdash & \{P_1 \land P_2\} \ c_1 \parallel c_2 \ \{Q_1 \land Q_2\} \end{array}$ 

- This rule is **not** compositional
- The specification of a program c is not just  $\{P\}_{\{Q\}}$ , but also all the intermediate assertions in the outline
- A change in one of the components may affect the proof, not only of the modified component, but also of all the others

- **Rely-Guarantee** is a well-known compositional method for proving Hoare logic properties of concurrent programs
- Rough idea: instead of trying to write interference-free proofs, explicitly account for the allowed interference
- No additional interference checks required
- Pioneered by Cliff Jones (1981, 1983)

# $R, G \vdash \{P\} \in \{Q\}$

- Pre-condition P(x)assertion describing initial state
- Rely condition R(x, x')
- Post-condition Q(x)

- relation describing atomic steps of environment assertion describing final state
- Guarantee condition G(x, x') relation describing atomic steps of the program

$$s_0 \xrightarrow{\mathsf{env}} s_1 \xrightarrow{\mathsf{prog}} s_2 \xrightarrow{\mathsf{env}} s_3 \xrightarrow{\mathsf{prog}} s_4 \xrightarrow{\mathsf{prog}} s_5 \xrightarrow{\mathsf{env}} s_6 \cdots s_{n-1} \xrightarrow{\mathsf{prog}} s_n$$

If  $P(s_0)$  and  $R(s_i, s_{i+1})$  for all  $s_i \xrightarrow{\text{env}} s_{i+1}$ , then  $G(s_i, s_{i+1})$  for all  $s_i \xrightarrow{\text{prog}} s_{i+1}$ , and  $Q(s_n)$  (the final state). Example

$$G_1 \equiv (x = 0 \land x' = 1) \lor (x = 2 \land x' = 3)$$
  
$$G_2 \equiv (x = 0 \land x' = 2) \lor (x = 1 \land x' = 3)$$

- Susan Owicki and David Gries: "An Axiomatic Proof Technique for Parallel Programs", Acta Informatica, 1976.
- Viktor Vafeiadis: "Modular fine-grained concurrency verification", PhD thesis, University of Cambridge, 2007.
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- Hossein Hojjat, Philipp Rümmer, Pavle Subotic, Wang Yi: "Horn Clauses for Communicating Timed Systems", HCVS 2014.